ABSTRACT

The dual bit split gate flash memory of the invention comprises a plurality of memory cells wherein each memory cell comprises a select gate overlying a substrate and isolated from the substrate by a select gate oxide layer, a first and second floating gate on opposite sidewalls of the select gate and isolated from the select gate by an oxide spacer, and a control gate overlying the select gate and the first and second floating gates and isolated from the select gate and the first and second floating gates by a dielectric layer, and source and drain regions within the substrate and shared by adjacent memory cells.